CLAIMS

What is Claimed is:

1. A semiconductor device having a non-volatile memory (NVM) array including rows and columns of memory cells comprising:

a first well region and a second well region within a semiconductor substrate, wherein the first well region and the second well region are spaced apart and electrically isolated;

a first column of memory cells positioned within the first well region;

a second column of memory cells positioned within the second well region;

a first tunnel dielectric of a first memory cell in the first column of memory cells and a second tunnel dielectric of a second memory cell in the second column of memory cells;

a first charge storage layer of the first memory cell formed over the first tunnel dielectric and a second charge storage layer of the second memory cell formed over the second tunnel dielectric;

a first control gate of the first memory cell formed over the first charge storage layer and a second control gate of the second memory cell formed over the second charge storage layer, wherein the first control gate and the second control gate are in a same row and electrically coupled via a common wordline;

a first bitline electrically coupled to drain regions of each memory cell in the first column of memory cells,

a second bitline electrically coupled to drain regions of each memory cell in the second column of memory cells;

a first source line electrically coupled to source regions of each memory cell in the first column of memory cells, wherein the first source line and a source region of at least one memory cell in the first column of memory cells is electrically coupled to the first well region; and

a second source line electrically coupled to source regions of each memory cell in the second column of memory cells, wherein the second source line, and a source region of at least one memory cell in the second column of memory cells is electrically coupled to the second well region.

2. The semiconductor device of claim 1, wherein the first and second well regions are p-wells.

3. The semiconductor device of claim 1, wherein the first and second memory cells are devoid of floating gates.

4. The semiconductor device of claim 1, wherein the first and second charge storage layers are non-conductive.

5. The semiconductor device of claim 4, wherein the first and second charge storage layers comprise nitrogen.

6. The semiconductor device of claim 5, wherein the first and second charge storage layers are selected from the group consisting of silicon nitride and silicon oxynitride.

7. The semiconductor device of claim 1, further comprising:

a first blocking layer of the first memory cell formed over the first charge storage layer and under the first control gate and a second blocking layer of the second memory cell formed over the second charge storage layer and under the first control gate.

8. The semiconductor device of claim 1, wherein the first well region and the second well region are spaced apart and electrically isolated by a trench isolation feature.

9. The semiconductor device of claim 8, further comprising a third well region below the trench isolation feature that electrically isolates the first well region from the second well region, wherein the first and second well regions have a polarity different than the third well region.

10. The semiconductor device of claim 1, wherein the first and second charge storage layers comprise discrete storage elements.

11. A semiconductor device having a non-volatile memory (NVM) array including rows and columns of memory cells comprising:

a well region formed within a semiconductor substrate;

a column of memory cells, wherein each memory cell comprises:

a source region and a drain region positioned within the well region, wherein each source region is electrically coupled to the well region;

a tunnel dielectric layer formed over the semiconductor substrate;

a charge storage layer formed over the tunnel dielectric layer; and

a control gate formed over the charge storage layer;

wordlines, wherein each wordline is electrically coupled to a respective control gate of a memory cell in the column of memory cells; and

a bitline electrically coupled to drain regions of each memory cell in column of memory cells.

12. The semiconductor device of claim 11, wherein each memory cell further comprises a blocking layer over the charge storing layer and under the control gate.

13. The semiconductor device of claim 11, wherein the charge storage layer comprises a semiconductor material.

14. The semiconductor device of claim 13, wherein the charge storage layer comprises discrete storage elements.

15. The semiconductor device of claim 11, wherein each column is devoid of conductive source lines that electrically couple to each source region.

16. The semiconductor device of claim 11, wherein the source region of each memory cell is silicided and electrically coupled to the well region by way of a silicided doped region, wherein the silicided doped region is doped the same polarity as the well.

17. The semiconductor device of claim 11, wherein the well region is p-type.

18. A semiconductor device comprising:

a semiconductor substrate comprising a first well region and a second well region, wherein the first well region and the second well region are isolated from each other;

a first memory cell formed in the first well region , wherein the first memory cell comprises:

a first source and a first drain region within the first well region having a polarity different than that of the first well region;

a first tunnel dielectric layer formed over the first source and the first drain region ;

a first charge storage layer formed over the first tunnel dielectric layer; and

a first control gate formed over the first charge storage layer; and

a second memory cell formed in the second well region , wherein the second memory cell comprises:

a second source and a second drain region within the second well region having a polarity different than that of the second well region;

a second tunnel dielectric layer formed over the second source and the second drain region ;

a second charge storage layer formed over the second tunnel dielectric layer;

a second control gate formed over the second charge storage layer; and

wherein the second memory cell and the first memory cell are electrically coupled via a wordline.

19. The semiconductor device of claim 18, wherein the first well region and the second well region are the same conductivity type and are p-type.

20. The semiconductor device of claim 18, wherein the first memory cell further comprises a first blocking layer over the first charge storage layer wherein the first charge storage layer is non-conductive.

21. The semiconductor device of claim 20, wherein the second memory cell further comprises a second blocking layer over the second charge storage layer wherein the second charge storage layer is non-conductive.

22. The semiconductor device of claim 18, wherein the second charge storage layer comprises nanocrystals.

23. A method for forming a non-volatile memory (NVM) array comprising:

forming a first well region and a second well region in a semiconductor substrate, wherein the first well region and the second well region are spaced apart by an isolation feature;

forming a first column of memory cells positioned within the first well region;

forming a second column of memory cells positioned within the second well region;

forming a first tunnel dielectric of a first memory cell in the first column of memory cells and a second tunnel dielectric of a second memory cell in the second column of memory cells;

forming a first charge storage layer of the first memory cell formed over the first tunnel dielectric and a second charge storage layer of the second memory cell formed over the second tunnel dielectric;

forming a first control gate of the first memory cell formed over the first charge storage layer and a second control gate of the second memory cell formed over the second charge storage layer, wherein the first control gate and the second control gate are in a same row and electrically coupled via a common wordline;

forming a first bitline, wherein the first bitline is electrically coupled to drain regions of each memory cell in the first column of memory cells;

forming a second bitline, wherein the second bitline is electrically coupled to drain regions of each memory cell in the second column of memory cells;

forming a first source line, wherein the first source line is electrically coupled to source regions of each memory cell in the first column of memory cells, and wherein the first source line and a source region of at least one memory cell in the first column of memory cells are electrically coupled to the first well region; and

forming a second source line, wherein the second source line is electrically coupled to source regions of each memory cell in the second column of memory cells, and wherein the second source line and a source region of at least one memory cell in the second column of memory cells are electrically coupled to the second well region.